REMARKS

The examiner's objections to the clams have all been met by appropriate amendment. Also, the abstract has been amended as required by the examiner. The examiner has rejected claims 1-8 and 10-12 under 35 U.S.C. 102(e) as being anticipated by Guo et al, U.S. Patent 6,606,273 B1, hereinafter Guo et al. This rejection is not thought to be well taken, especially in view of the amendments to claim 1, the only independent claim in the application.

Before discussing the claims and the Guo et al reference in detail, it is believed that an overview of the present invention and the teachings of Guo at al would be helpful.

The description in Guo et al, in part, indicates that the test structures are an FET device and a capacitor fabricated near to each other for the purposes of characterizing the components of the Flash devices (represented as the combination of a capacitor manufactured directly above an FET device). The main difference between Guo et al and applicant's invention is that in Guo et al the test capacitor has only a single contact point to each plate; upper (polysilicon gate) and lower (substrate), so an applied voltage would be the same across the plate. These are biased differently according to the particular function being performed.

The present invention teaches a method wherein a target voltage is determined by a first ramp - unitary voltage across the top and bottom plates. This is followed by a test where a voltage difference is established across the top plate (one voltage is slightly above the target voltage) to produce a series current, which in turn produces a voltage distribution across the top plate. This voltage distribution leads to varying degrees of tunneling currents across the structure. The idea is to be able to localize and measure the more severe tunneling sites for subsequent analysis (indicated by more severe steps in measured tunneling leakage). Thus,

applicant's method will reveal and allow measurement of tunneling variations across the test piece, whereas the Guo et al teaching does not allow or provide for such.

Turning now to claim 1, the only independent claim in the application, this claim as amended specifically requires determining a target voltage, applying a voltage above the target voltage to the first end of the second plate, applying a voltage to the second end of the second plate, and incrementally changing the voltage level at the second end of the second plate to change the length of the capacitive structure above the target voltage to localize and measure tunneling leakage at selected locations along the capacitor. This is not taught nor suggested by Guo et al, since Guo et al cannot change the length of the capacitor. They can only measure the average leakage at various conditions. Thus, claim 1 clearly distinguishes over Guo et al.

Prior art is anticipatory only if every element of the claimed invention is disclosed in a single item of prior art in the form literally defined in the claim. Jamesbury Corp. v. Litton Indus. Products, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); Atlas Powder Co. v. du Pont, 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984); American Hospital Supply v. Travenol Labs, 745 F.2d 1, 223 USPQ 577 (Fed. Cir. 1984).

"Anticipation requires identity of the claimed process and a process of the prior art; the claimed process, including each step thereof, must have been described or embodied, either expressly or inherently, in a single reference" Glaverbel Societe Anonyme v. Northlake Marketing & Supply, Inc., 45 F. 3d 1550, 1554, 33 USPQ2d 1496, 1498 (Fed. Cir. 1995).

Clearly, those steps in claim 1 that call for varying the voltage along the length of the capacitor to localize and measure tunneling along the length of the capacitor are not disclosed or suggested in Guo et al and, thus, claim 1 is clearly allowable.

Claims 2-8 and 10-12 are dependent, directly or indirectly, on claim 1 and, for the same reasons, are believed to be allowable.

With respect to claim 4, it is submitted that the voltage is not varied to correspond with the segments of the plate but, rather, as described above, to emulate various functions (e.g. device cycles). Thus, for this additional reason, claim 4 is believed to be allowable.

Claims 5 and 6 relate to how the voltage applied to the second end of the second plate is incrementally increased or decreased. Since Guo et al do not apply a voltage to the second end of the second plate and then incrementally change it, they cannot anticipate these claims. Thus, claims 5 and 6 are clearly allowable.

With respect to claim 10, this requires that the tunneling voltage be measured at each segment. This is clearly not taught nor suggested by Guo et al and, thus, for this additional reason, claim 19 is clearly allowable.

Claim 11 requires that the voltage between plates be measured with a differential amplifier. Since the voltage between plates is not measured, it could not be measured with a differential amplifier. Thus, for this additional reason, claim 11 is believed to be allowable.

Claim 9 has been rejected under 35 U.S.C. 103(a) as being anticipated by Guo et al. This rejection is not thought to be well taken. First, claim 9 is dependent upon claim 1 and, for the same reasons, is believed to be allowable. Moreover, and as acknowledged by the examiner, Guo et al do not teach or suggest one element of claim 9. Since all of the elements are not taught, claim 9, for this additional reason, is believed to be allowable.

In view of the above, it is believed that each of the claims in the application is distinguishable, one from the other, and over the prior art. Therefore, reconsideration and allowance of all of the claims is respectfully requested.

Respectfully submitted,

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